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For: INTEGRATED DIGITAL CALIBRATION CIRCUIT AND DIGITAL TO ANALOG CONVERTER (DAC)

1 1. An integrated programmable digital calibration circuit and digital to
2 analog converter comprising:
3 a digital to analog converter (DAC); and
4 a digital calibration circuit including a memory for storing predetermined
5 end point coefficients of said digital to analog converter transfer function; and an
6 arithmetic logic unit for applying the end point coefficients to the DAC input signal to
7 adjust the end points of said DAC.

1 2. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 1 in which said end point coefficients include the offset
3 coefficient and gain coefficient.

1 3. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 2 in which said arithmetic logic unit includes an arithmetic
3 circuit having a multiplier circuit for multiplying the DAC input by the gain coefficient
4 and an adder circuit for adding the offset coefficient to said input signal.

1 4. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 3 in which said arithmetic circuit includes a divider circuit for
3 dividing the product of the DAC input and the gain coefficient before adding it to the
4 offset coefficient.

1 5. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 3 in which said arithmetic circuit includes a second adder for
3 combining a second constant with the gain coefficient before it is multiplied by the DAC
4 input.

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6 6. The integrated programmable digital calibration circuit and digital to
7 analog converter of claim 1 in which said of said end point coefficients include the zero
8 scale and full scale coefficients.

1 7. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 6 in which said arithmetic logic unit includes an arithmetic
3 circuit for algebraically counting the zero scale output and ideal output and normalizing
4 them by the least significant bit (LSB) value to obtain the zero scale coefficient and
5 combining the full scale output and ideal output and normalizing them by the LSB to
6 obtain the full scale coefficient and applying those coefficients to the input signal to the
7 DAC.

1 8. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 1 in which said digital calibration circuit and DAC are on the
3 same integrated circuit chip.

1 9. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 8 in which said memory is in said digital calibration circuit.

1 10. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 8 in which said memory is external to said digital calibration
3 circuit.

1 11. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 8 in which said memory is a user accessible programmable
3 memory.

1 12. A programmable digital calibration system including an integrated digital
2 calibration circuit and digital to analog converter comprising:
3 a digital to analog converter (DAC);
4 an analog signal circuit responsive to said DAC; and
5 a digital calibration circuit including a memory for storing the predetermined end
6 point coefficients of said DAC transfer function; and an arithmetic logic unit for
7 applying the end point coefficients to the DAC input signal to adjust for the end points of
8 said DAC and said analog signal circuit.

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1 13. The programmable digital calibration system including an integrated
2 digital calibration circuit and digital to analog converter of claim 12 in which said digital
3 calibration circuit and DAC are on the same integrated circuit chip.

1 14. The programmable digital calibration system including an integrated
2 digital calibration circuit and digital to analog converter of claim 13 in which said
3 memory is in said digital calibration circuit.

1 15. The programmable digital calibration system including an integrated
2 digital calibration circuit and digital to analog converter of claim 13 in which said
3 memory is external to the digital calibration circuit.

1 16. The programmable digital calibration system including an integrated
2 digital calibration circuit and digital to analog converter of claim 13 in which said
3 memory is a user accessible programmable memory.

1 17. A programmable integrated digital calibration circuit and digital to analog
2 converter comprising:

3 a digital to analog converter; and
4 a digital calibration circuit including a memory for storing the predetermined
5 offset coefficient and gain coefficient of said digital to analog converter (DAC) and an
6 arithmetic logic unit including an arithmetic circuit having a multiplier circuit for
7 multiplying the DAC input by the gain coefficient and an adder circuit for adding the
8 offset coefficient to said input signal to adjust the gain and offset of said DAC.

1 18. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 17 in which said arithmetic circuit includes a divider circuit for
3 dividing the product of the DAC input and the gain coefficient before adding it to the
4 offset coefficient.

1 19. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 17 in which said arithmetic circuit includes a second adder for
3 combining a second constant with the gain coefficient before it is multiplied by the DAC
4 input.

1 20. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 17 in which said digital calibration circuit and DAC are on the
3 same integrated circuit chip.

1 21. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 18 in which said memory is in said digital calibration circuit.

1 22. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 18 in which said memory is external to said digital calibration
3 circuit.

1 23. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 18 in which said memory is a user accessible programmable
3 memory

1 24. A programmable digital calibration system including a integrated digital
2 calibration circuit and digital to analog converter comprising:
3 a digital to analog converter (DAC);
4 an analog signal circuit responsive to said DAC; and
5 a digital calibration circuit including a memory for storing the predetermined
6 offset coefficient and gain coefficient of said DAC and said analog signal circuit; and an
7 arithmetic logic unit including an arithmetic circuit having a multiplier circuit for
8 multiplying the DAC input by the gain coefficient and an adder circuit for adding the
9 offset coefficient to said input signal to adjust the gain and offset of said DAC and said
10 analog signal circuit.

1 25. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 24 in which said arithmetic circuit includes a divider circuit for
3 dividing the product of the DAC input and the gain coefficient before adding it to the
4 offset coefficient.

1 26. The integrated programmable digital calibration circuit and digital to
2 analog converter of claim 24 in which said arithmetic circuit includes a second adder for
3 combining a second constant with the gain coefficient before it is multiplied by the DAC
4 input.

1 27. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 24 in which said digital calibration circuit and DAC are on the

3 same integrated circuit chip.

1 28. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 24 in which said memory is in said digital calibration circuit.

1 29. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 24 in which said memory is external to said digital calibration
3 circuit.

1 30. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 24 in which said memory is a user accessible programmable
3 memory.

1 31. A programmable integrated digital calibration circuit and digital to analog
2 converter comprising:
3 · a digital to analog converter (DAC); and
4 · a digital calibration circuit including a memory for storing predetermined zero
5 scale and full scale coefficients of said digital to analog converter (DAC) and an
6 arithmetic logic unit including an arithmetic circuit for algebraically combining the zero
7 scale output and ideal output and normalizing them by the least significant bit (LSB)
8 value to obtain the zero scale coefficient and combining the full scale output and ideal
9 output and normalizing them by the LSB to obtain the full scale coefficient and applying
10 those coefficients to the input signal to the DAC to adjust the zero scale and full scale of
11 said DAC.

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1 32. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 31 in which said digital calibration circuit and DAC are on the
3 same integrated circuit chip.

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1 33. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 32 in which said memory is in said digital calibration circuit.

1 34. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 32 in which said memory is external to said digital calibration
3 circuit.

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1 35. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 32 in which said memory is a user accessible programmable
3 memory.

1 36. A programmable digital calibration system including an integrated digital
2 calibration circuit and digital to analog converter comprising:
3 a digital to analog converter (DAC);
4 an analog or mixed signal circuit responsive to said DAC; and
5 a digital calibration circuit including a memory for storing predetermined zero
6 scale and full scale coefficients of said DAC and said analog signal circuit; and an
7 arithmetic logic unit including an arithmetic circuit for algebraically combining the zero
8 scale output and ideal output and normalizing them by the least significant bit (LSB)
9 value to obtain the zero scale coefficient and combining the full scale output and ideal
10 output and normalizing them by the LSB to obtain the full scale coefficient and applying
11 those coefficients to the input signal of the DAC to adjust for the zero scale and full
12 scale offsets of said DAC and said analog signal circuit.

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1 37. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 36 in which said digital calibration circuit and DAC are on the
3 same integrated circuit chip.

1 38. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 37 in which said memory is in said digital calibration circuit.

1 39. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 37 in which said memory is external to said digital calibration
3 circuit.

1 40. The programmable integrated digital calibration circuit and digital to
2 analog converter of claim 37 in which said memory is a user accessible programmable
3 memory.

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2 41. An integrated digital calibration circuit and digital to analog converter
3 comprising:
4 a digital to analog converter (DAC); and
5 a digital calibration circuit including a memory for storing predetermined
6 complements of the end point errors of said digital to analog converter transfer function;
7 and an arithmetic logic unit for applying the complements of the end point errors to the
8 DAC input signal to compensate for the end point errors of said DAC.

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1 42. The integrated digital calibration circuit and digital to analog converter of
2 claim 41 in which said complements of said end point errors include the offset error
3 coefficient and gain error coefficient.

1 43. The integrated digital calibration circuit and digital to analog converter of
2 claim 42 in which said arithmetic logic unit includes an arithmetic circuit having a
3 multiplier circuit for multiplying the DAC input by the gain error coefficient and an adder
4 circuit for adding the offset error coefficient to said input signal.

1 44. The integrated digital calibration circuit and digital to analog converter of
2 claim 41 in which said complement of said end point errors includes the zero scale and
3 full scale error coefficients.

1 45. The integrated digital calibration circuit and digital to analog converter of

2 claim 44 in which said arithmetic logic unit includes an arithmetic circuit for
3 algebraically counting the zero scale output and ideal output and normalizing them by the
4 least significant bit (LSB) value to obtain the zero scale error coefficient and combining
5 the full scale output and ideal output and normalizing them by the LSB to obtain the full
6 scale error coefficient and applying those error coefficients to the input signal to the
7 DAC.

1 46. The integrated digital calibration circuit and digital to analog converter of
2 claim 41 in which said digital calibration circuit and DAC are on the same integrated
3 circuit chip.

1 47. The integrated digital calibration circuit and digital to analog converter of
2 claim 46 in which said memory is in said digital calibration circuit.

1 48. The integrated digital calibration circuit and digital to analog converter of
2 claim 46 in which said memory is external to said digital calibration circuit.

1 49. The integrated digital calibration circuit and digital to analog converter of
2 claim 46 in which said memory is a user accessible programmable memory.

1 50. A digital calibration system including an integrated digital calibration
2 circuit and digital to analog converter comprising:
3 a digital to analog converter (DAC);
4 an analog signal circuit responsive to said DAC; and
5 a digital calibration circuit including a memory for storing the predetermined
6 complement of the end point error of said DAC transfer function; and an arithmetic logic
7 unit for applying the complements of the end point errors to the DAC input signal to
8 compensate for the end point errors of said DAC and said analog signal circuit.

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1 51. The digital calibration system integrated digital calibration circuit and
2 digital to analog converter of claim 50 in which said digital calibration circuit and DAC
3 are on the same integrated circuit chip.

1 52. The digital calibration system integrated digital calibration circuit and
2 digital to analog converter of claim 51 in which said memory is in said digital calibration
3 circuit.

1 53. The digital calibration system integrated digital calibration circuit and
2 digital to analog converter of claim 51 in which said memory is external to said digital
3 calibration circuit.

1 54. The digital calibration system integrated digital calibration circuit and

2 digital to analog converter of claim 51 in which said memory is a user accessible
3 programmable memory.

1 55. An integrated digital calibration circuit and digital to analog converter
2 comprising:
3 a digital to analog converter; and
4 a digital calibration circuit including a memory for storing the predetermined
5 offset error coefficient and gain error coefficient of said digital to analog converter (DAC)
6 and an arithmetic logic unit including an arithmetic circuit having a multiplier circuit for
7 multiplying the DAC input by the gain error coefficient and an adder circuit for adding
8 the offset error coefficient to said input signal to compensate for the gain and offset errors
9 of said DAC.

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1 56. The integrated digital calibration circuit and digital to analog converter of
2 claim 55 in which said digital calibration circuit and DAC are on the same integrated
3 circuit chip.

1 57. The integrated digital calibration circuit and digital to analog converter of
2 claim 56 in which said memory is in said digital calibration circuit.

1 58. The integrated digital calibration circuit and digital to analog converter of
2 claim 55 in which said memory is external to said digital calibration circuit.

1 59. The integrated digital calibration circuit and digital to analog converter of
2 claim 55 in which said memory is a user accessible programmable memory.

1 60. A digital calibration system including a integrated digital calibration
2 circuit and digital to analog converter comprising:
3 a digital to analog converter (DAC);
4 an analog signal circuit responsive to said DAC; and
5 a digital calibration circuit including a memory for storing the predetermined
6 offset error coefficient and gain error coefficient of said DAC and said analog signal
7 circuit; and an arithmetic logic unit including an arithmetic circuit having a multiplier
8 circuit for multiplying the DAC input by the gain error coefficient and an adder circuit for
9 adding the offset error coefficient to said input signal to compensate for the gain and
10 offset error of said DAC and said analog signal circuit.

1 61. The integrated digital calibration circuit and digital to analog converter of
2 claim 60 in which said digital calibration circuit and DAC are on the same integrated
3 circuit chip.

1 62. The integrated digital calibration circuit and digital to analog converter of
2 claim 61 in which said memory is in said digital calibration circuit.

1 63. The integrated digital calibration circuit and digital to analog converter of
2 claim 61 in which said memory is external to said digital calibration circuit.

1 64. The integrated digital calibration circuit and digital to analog converter of
2 claim 61 in which said memory is a user accessible programmable memory.

1 65. An integrated digital calibration circuit and digital to analog converter
2 comprising:
3 a digital to analog converter (DAC); and
4 a digital calibration circuit including a memory for storing predetermined zero
5 scale and full scale error coefficients of said digital to analog converter (DAC) and an
6 arithmetic logic unit including an arithmetic circuit for algebraically combining the zero
7 scale output and ideal output and normalizing them by the least significant bit (LSB)
8 value to obtain the zero scale error coefficient and combining the full scale output and
9 ideal output and normalizing them by the LSB to obtain the full scale error coefficient
10 and applying those error coefficients to the input signal to the DAC to compensate for the
11 zero scale and full scale errors of said DAC.

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1 66. The integrated digital calibration circuit and digital to analog converter of
2 claim 65 in which said digital calibration circuit and DAC are on the same integrated
3 circuit chip.

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1 67. The integrated digital calibration circuit and digital to analog converter of
2 claim 66 in which said memory is in said digital calibration circuit.

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1 68. The integrated digital calibration circuit and digital to analog converter of
2 claim 66 in which said memory is external to said digital calibration circuit.

1 69. The integrated digital calibration circuit and digital to analog converter of
2 claim 66 in which said memory is a user accessible programmable memory.

1 70. A digital calibration system including an integrated digital calibration
2 circuit and digital to analog converter comprising:
3 a digital to analog converter (DAC);
4 an analog or mixed signal circuit responsive to said DAC; and
5 a digital calibration circuit including a memory for storing predetermined zero
6 scale and full scale error coefficients of said DAC and said analog signal circuit; and an
7 arithmetic logic unit including an arithmetic circuit for algebraically combining the zero
8 scale output and ideal output and normalizing them by the least significant bit (LSB)
9 value to obtain the zero scale error coefficient and combining the full scale output and
10 ideal output and normalizing them by the LSB to obtain the full scale error coefficient
11 and applying those error coefficients to the input signal of the DAC to compensate for the
12 zero scale and full scale offset errors of said DAC and said analog signal circuit.

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1 71. The integrated digital calibration circuit and digital to analog converter of
2 claim 70 in which said digital calibration circuit and DAC are on the same integrated
3 circuit chip.

1 72. The integrated digital calibration circuit and digital to analog converter of
2 claim 71 in which said memory is in said digital calibration circuit.

1 73. The integrated digital calibration circuit and digital to analog converter of
2 claim 71 in which said memory is external to said digital calibration circuit.

1 74. The integrated digital calibration circuit and digital to analog converter of
2 claim 71 in which said memory is a user accessible programmable memory.